REMARKS

The present application was filed on December 8, 2000 with claims 1-17. Claim 3 is canceled herein. Claims 1, 2 and 4-17 remain pending.

Applicant respectfully requests reconsideration of the present application in view of the above amendments and the following remarks.

Claims 1, 2, 4, 9, 10, 12 and 14-17 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,257,218 (hereinafter "Poon"). Claims 11 and 13 stand rejected under 35 U.S.C. §103(a) as being obvious over Poon. Claims 5-8 are allowed. Claim 3 is indicated as containing allowable subject matter.

Applicant respectfully traverses the §102(b) and §103(a) rejections.

With regard to the §102(b) rejection, Applicant notes that the Manual of Patent Examining Procedure (MPEP), Eight Edition, August 2001, §2131, specifies that a given claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the "identical invention . . . in as complete detail as is contained in the . . . claim," citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

For the reasons identified below, Applicant submits that the Examiner has failed to establish anticipation of at least independent claims 1, 16 and 17 by the Poon reference.

The present invention as set forth in claim 1 as originally filed is directed to an adder having a plurality of computational stages each associated with one or more bit positions of the adder, with the plurality of computational stages including one or more computational stages for generating a sum output signal and a primary carry-output signal of the adder. The adder further includes a flag generation circuit coupled to at least one signal line of at least one of the computational stages and operative to generate an overflow flag for the adder, the overflow flag being generated substantially in parallel with the generation of at least one of the sum output signal and the primary carry-output signal of the adder.

An illustrative embodiment of the claimed arrangement advantageously provides a substantial reduction in the computational delay associated with generation of an overflow flag, "without requiring any significant increase in the transistor count or circuit area of the adder, and thus without increasing adder cost or complexity" (Specification, page 7, lines 3-10).

It is believed that the Poon reference fails to meet the limitations of independent claim 1 as originally filed, and fails to provide the associated advantages.

In formulating the §102(b) rejection, the Examiner relies on the disclosure in column 13, lines 9-12 of Poon, which states that a primary carry-output signal C_{N-1} of the FIG. 13 adder is available at the output of the adder as "an overflow bit" utilizable for "extending the number of bits in the operands A and B." The Examiner thus apparently argues that the primary carry-output signal C_{N-1} in the Poon adder reads on the overflow flag as claimed. Applicant respectfully disagrees. Use of the primary carry-output signal itself as an overflow bit in the manner disclosed in Poon fails to meet the above-recited limitations of claim 1.

Independent claims 16 and 17 include limitations similar to those of claim 1, and are believed allowable for substantially the same reasons identified above with regard to claim 1.

Dependent claims 2-4 and 9-15 are believed allowable for at least the reasons identified above with regard to claim 1. Moreover, these claims are believed to define additional separately-patentable subject matter over Poon and the other art of record.

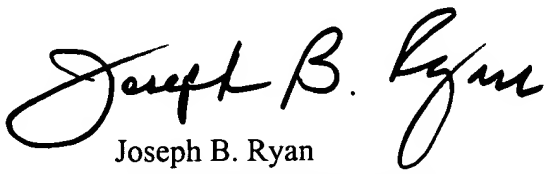
The §102(b) and §103(a) rejections are therefore respectfully traversed.

Notwithstanding the foregoing traversal, Applicant has amended each of independent claims 1, 16 and 17 to incorporate the limitations of dependent claim 3, which as noted above has been indicated as containing allowable subject matter.

In view of the traversal, Applicant submits that the amendments to claims 1, 16 and 17 are not made for reasons relating to patentability over Poon or any other art of record, but instead are made solely in order to expedite prosecution of the application.

Accordingly, Applicant believes that claims 1-17 as amended are in condition for allowance, and respectfully requests the withdrawal of the §102(b) and §103(a) rejections.

Respectfully submitted,



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